

REMARKS

A. Specification

In the Office Action, paragraph [0022] was objected to because of certain minor informalities. Applicant has herein amended paragraph [0022], in line 5, to change “10” to “32” when referring to the VCO, as suggested in the Office Action. Line 3 of paragraph [0022] has also been amended to make this change.

Applicant has not, however, changed “31” to “30” in lines 1 and 6 of paragraph [0022] as suggested in the Office Action when referring to the PLL because reference number “31” is used throughout the application when referring to the PLL. Reference number “30” is used in the application to refer to the frequency synthesizer (e.g., the combination of the PLL 31 and the auxiliary digital frequency detector 50 and other components). *See* Figure 2. Therefore, Applicant submits that this requested change is unnecessary.

By this amendment, the Applicant has also corrected various other minor clerical errors in the application.

B. Claims

In the Office Action, claims 1-3, 5, 16, 17 and 19 were rejected under 35 U.S.C. § 102(e) as being anticipated by published U.S. patent application Pub. No. 2004/0223575 to Meltzer et al. Claims 4 and 18 were rejected as being obvious under 35 U.S.C. § 103(a) over Meltzer in view of U.S. Pat. 6,359,476 to Hartman et al. Claims 6-15 were objected to as dependent upon a rejected base claim. Applicant traverses the rejections as follows.

1. Claims 2-15 and 20

Applicant has canceled rejected independent claim 1 and has amended claim 2 to now be in independent form. As now amended, claim 2 recites a phase locked loop and an auxiliary digital frequency detector. The phase locked loop comprises an analog mixer phase detector, a programmable divider, a loop filter and a voltage controlled oscillator. Claim 2 further recites that the auxiliary digital frequency detector includes “an output terminal coupled to a second input terminal of the loop filter” of the phase locked loop.

The Meltzer reference does not disclose or suggest all of the elements of amended claim 2. Meltzer discloses a frequency synthesizer having two loops: an analog loop and a digital loop. The Office Action identifies the “digital frequency difference detector 15” of Meltzer, which is part of Meltzer’s digital loop, as the claimed auxiliary digital frequency detector. In Meltzer, however, the digital frequency difference detector 15 is not coupled to the loop filter of the phase locked loop, which is in the analog loop of Meltzer’s design. Rather, the digital frequency difference detector 15 is coupled to the VCO 11 in Meltzer for the purpose of controlling the center frequency of the VCO. See Meltzer, Figure 1 and paragraph [0014].

This is fundamentally different from the frequency synthesizer claimed in claim 2 of the present application. Although it has been known for some time that analog mixers can be used as phase detectors, they are not widely used in PLL circuits because of their inability to acquire phase lock. In the frequency synthesizer of claim 2, however, the auxiliary digital frequency detector detects the frequency error when the PLL is out of lock and, as a result, causes a “steering current” to flow into or out of the loop filter of the PLL. This in turn causes the voltage applied to the VCO by the loop filter to ramp up or down at a rate set by a time constant of the loop filter. When the VCO reaches a frequency such that the output signal from the analog phase

mixer detector is within the bandpass range of the loop filter, phase lock for the PLL is achieved. Thus, the auxiliary digital phase detector of claim 2, by being coupled to an input terminal of the loop filter to provide the steering current to the loop filter when the PLL is out of lock, allows an analog phase mixer detector to be used in the PLL. This is an important potential benefit because frequency detectors implemented as analog mixers can provide excellent phase noise performance.

Therefore, claim 2, as well as claims 3-15 depending therefrom, are not anticipated by or obvious in view of Meltzer and are in condition for allowance.

New dependent claim 20 has also been added. By virtue of its dependence on claim 2, Applicant submits that claim 20 is also in condition for allowance.

2. Claims 16 and 18

Independent claim 16 has been amended to clarify that the “means making the analog mixer phase detector automatically acquire phase lock when the phase locked loop is out of lock” is coupled to the loop filter of the phase locked loop. For reasons analogous to those stated above with respect to claim 2, Applicant submits that claim 16 is not anticipated by Meltzer.

Claim 17 has been canceled and claim 18 has been amended to depend from claim 16 rather than canceled claim 17. For at least the reason that claim 18 depends from claim 16, claim 18 is also in condition for allowance.

3. Claim 19

Claim 19 has been amended to clarify that the method includes adjusting the voltage applied to the voltage controlled oscillator from the loop filter “by providing a current to a timing capacitor of the loop filter to cause the voltage supplied to the voltage controlled oscillator to

change based on a time constant of the loop filter.” For reasons analogous to those stated above with respect to claim 2, claim 19 is not anticipated by Meltzer.

The dependent claims of the present application recite further distinctions when compared with the cited prior art. A detailed discussion of these differences is believed to be unnecessary at this time in view of the basic differences in the independent claims pointed out above. Applicant is not otherwise conceding the correctness of the rejections with respect to any of the dependent claims in the application and hereby reserves the right to make additional arguments as may be necessary because additional features of the claims further distinguish the claims from the cited references, taken alone or in combination.

C. Drawings

Although not objected to in the Office Action, Figure 4 has been amended to correct a clerical error. The operational amplifier that is part of the loop filter 42 should have the reference number “82”, not “80”.

CONCLUSION

In view of the above, Applicant respectfully requests withdrawal of the rejections and allowance of the claims. If the Examiner is of the opinion that the instant application is in condition for disposition other than allowance, the Examiner is respectfully requested to the

undersigned attorney at the telephone number listed below in order that the Examiner's concerns may be expeditiously addressed.

Respectfully submitted,

Date: July 5, 2005



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ANNOTATED SHEET SHOWING CHANGES

Frequency Synthesizer having PLL with an Analog Phase Detector

Serial No. 10/713,717
Response to Office Action mailed April 13, 2005

Block diagram of a DDS-based frequency synthesizer with a lock detection circuit. The diagram shows the following components and connections:

- VCO:** A voltage-controlled oscillator with output 32.
- Reference Signal:** Input to the DDS and the lock detection logic.
- Prescaler:** A block with output 36, connected to the DDS and the lock detection logic.
- DDS:** A digital-to-sine converter with output 70, connected to the Prescaler and the lock detection logic.
- BALUN:** A transformer with output 46, connected to the DDS and the lock detection logic.
- BPF:** A bandpass filter with output 48, connected to the DDS and the lock detection logic.
- Loop Signal:** A mixer with output 40, connected to the DDS and the lock detection logic.
- Output Signal:** A signal path with output 92.
- Lock Detection Logic:**
 - Inputs: DDS output 70, DDS output 52, DDS output 44, DDS output 72, DDS output 76, DDS output 54, DDS output 62, DDS output 60, DDS output 64, and Reference Signal.
 - Outputs: Command, COMP SIGNAL, and Lock.
 - Logic: An XOR gate (NC7S286) and a NAND gate (64).

Annotations in the diagram:

- Reference Number Corrected:** A handwritten note pointing to the reference signal input.
- 82:** A handwritten note pointing to the DDS output 82.
- 50:** A handwritten note pointing to the reference signal input.
- 90:** A handwritten note pointing to the DDS output 90.